In re Application of:
Rana P. Singh
Serial No.: 10/045913
Filed: January 9, 2002
For: SEMICONDUCTOR DEVICE STRUCTURE AND METHOD FOR FORMING

April 28, 2004

Art Unit: 2811
Examiner: Samuel A. Gebremariam
Docket No.: SC11448TP-P01

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
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Pat Thomas 4-28-04
SIGNATURE DATE

COMMISSIONER OF PATENTS AND TRADEMARKS
ALEXANDRIA, VA 22313-1450

BOARD OF PATENT APPEALS & INTERFERENCES:

Responsive to the Office Action dated January 28, 2004, Applicants hereby request reinstatement of the appeal on the above referenced application. A supplemental appeal brief in triplicate is attached.

Respectfully submitted,

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Freescale Semiconductor, Inc.
A Motorola Subsidiary
Customer No.: 23125

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

COMMISSIONER OF PATENTS AND TRADEMARKS
ALEXANDRIA, VA 22313-1450

BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed pursuant to 37 C.F.R. §1.192 in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. Applicants believe no charges are due with this brief. If Applicant has overlooked any fees, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

REAL PARTY IN INTEREST

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003.

RELATED APPEALS AND INTERFERENCES

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003.

STATUS OF CLAIMS

Claims 1-10, 15-34, and 38-42 are the subject of this appeal. Claims 1-10, 15-34, and 38-42 were presented to the USPTO for the first time on January 9, 2002, the filing date of the present application. [Note: The present application is a continuation in part of U.S. patent application (09/997,145).] In a first Office Action, the Examiner issued a restriction requirement between device claims 11-14 and 35-37 and process claims 1-10, 15-34, and 38-42. Appellants responded by electing process claims 1-10, 15-34, and 38-42, with traverse. In a second Office Action, the Examiner rejected claims 1-3, 5, 8-10, 15, 19, 23-27, and 29 under 35 USC 102 (e) as being anticipated by Shiozawa et al. (US Patent 6,245,641), rejected claims 4, 6, 16, 17, 18, 22, 28, 32, 40, and 42 under 35 USC 103(a) as being unpatentable over the same reference, and rejected claims 7, 18, 20, and 21 under 35 USC 103(a) as being unpatentable over Shiozawa in view of Lee (US Patent 5,994,201), and rejected claims 38-42 under 35 USC 103(a) as being unpatentable over Shiozawa in view of Koike (US Patent 5,578,518). Appellants responded to the rejection with arguments and cancelled non-elected claims 11-14 and 35-37. In this response, Appellants also amended claims 1, 5, 15, 19, 20, 26, and 29. The Examiner finally rejected the claims on the same grounds as originally rejected. Appellants responded in an after final response with arguments. At this point, claims 1-10, 15-34, and 38-42 were still pending. The Examiner did not find Appellants'

arguments persuasive. Thus, Appellants submitted a Notice of Appeal on July 22, 2003, and submitted an Appeal Brief in support of the Notice of Appeal on October 22, 2003. The Examiner reopened prosecution and mailed an office action on January 28, 2004. This Supplemental Brief is being submitted in response to the Examiner's reopening of prosecution.

STATUS OF AMENDMENTS

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003.

SUMMARY OF THE INVENTION

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003.

ISSUES

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003.

GROUPING OF CLAIMS

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003. As a reminder, the groupings are as follows:

Group A → Claims 1-10 and 15-28
Group B → Claims 29-34 and 38-42

ARGUMENTS

This section is incorporated by reference from Appellants' previously filed Appeal Brief submitted October 22, 2003, since all of this section in the previously filed Appeal Brief is still applicable. In addition, Appellants are including herein arguments which are relevant to the new ground(s) of rejection raised in the Office Action that reopened prosecution.

In the Office Action that reopened prosecution mailed January 28, 2004, the Examiner "takes the position that growing an oxide layer is the same as depositing." (See the Response to Arguments section of the January 28, 2004, Office Action.) The Examiner proceeds to cite Merriam-Webster's Collegiate Dictionary (2001), Tenth Edition, which defines grow as "to increase in size by assimilation of material into the living organism or by accretions of material in a non-biological process." The Examiner then concludes that "since deposition process results in accretion of material, the two processes are the same." However, Appellants disagree and submit that the Examiner is incorrectly applying a non-technical definition to a technical term.

Firstly, Appellants will reiterate the argument presented in the previously filed Appeal Brief. Appellants respectfully submit that the Examiner's statement that "growing an oxide layer is the same as depositing an oxide layer" is incorrect. Growing is not the same as depositing an oxide layer. For example, a grown oxide generally results in a higher quality oxide as compared to a deposited oxide. Also, a grown oxide may be better able to achieve other benefits such as corner rounding. Furthermore, it may not be possible to grow an oxide. For example, the high temperature required in growing the oxide may damage other portions of the wafer, or there may not be a suitable material on which to grow the oxide. Therefore, there are many situations in which one form of an oxide (grown or deposited) is preferable or required over the other. For example, as discussed in the previously filed Appeal Brief, silicon oxide film 8 of Shiozawa cannot be grown since it must also be formed on the silicon nitride films 3a and 3d in order to prevent corner erosion of the nitride films 3a and 3b during the trench fill process (see col. 10, lines 5-10 and lines 45-65, of Shiozawa). Therefore,

growing silicon oxide film 8 would destroy the functionality of Shiozawa because the silicon oxide would not grow on silicon nitride films 3a and 3d which is necessary in order for the structure of Shiozawa to operate properly. Therefore, in this example, a situation exists in which a grown oxide is not possible.

Appellants, in the previously filed Appeal Brief, also provided (as Exhibit A) an excerpt (pp. 109-110) from the book "*Silicon Processing for the VLSI Era*," by S. Wolf and R.N. Tauber which is intended to provide further support that growing and depositing layers is not the same in the context of semiconductor processing. This excerpt divides the formation of thin films into two separate groups: 1) film growth by *interaction of a vapor-deposited species with the substrate* (this category includes thermal oxidation); and 2) film formation by deposition *without causing changes to the substrate material* (this category includes CVD). That is, film growth and film deposition are different processes which affect the substrate differently (the former interacts with the substrate while the latter does not cause changes to the substrate material). Therefore, it is incorrect for the Examiner to state that growing an oxide layer is the same as depositing an oxide layer.

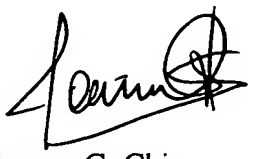
Referring back to the January 28, 2004, Office Action that reopened prosecution, Appellants submit that the Examiner incorrectly relies on a non-technical dictionary definition rather than relying on the usage of depositing and growing as understood by persons skilled in the relevant art, which, in this case, is semiconductor processing. Firstly, in construing claims, the focus begins with the language of the claims themselves. See *The Dow Chemical Company v. Sumitomo Chemical Company, Ltd. and Sumitomo Chemical America, Inc.*, 257 F.3d 1364, 1372 (Fed. Cir. 2001). For example, in each of the independent claims of Groups A and B, Appellants chose to use the word "growing" in describing "growing the first insulator liner" rather than the word "forming" (which can broadly be construed to include growing or depositing) or the word "depositing". Furthermore, in some claims, such as claim 1, Appellants claim "growing a first insulator liner" and "depositing an insulating layer." That is, one element uses "growing" and the other "depositing" where the two words were chosen to convey different meanings. If growing and depositing are taken to be the same, then this

distinction in claim 1 would be erased. Furthermore, the specification also treats the two terms "growing" and "depositing" differently. For example, the specification describes growing with respect to the insulator liners (such as, for example, liners 22 and 24 of the current Application) and describes depositing with respect to the insulating layer (such as, for example, trench fill layer 30). Therefore, the terms growing and depositing are also used differently within the specification, and thus cannot be considered the same.

Secondly, the claims need to be construed as understood by persons skilled in the relevant art. See *Dow Chemical*, 257 F.3d at 1372. In this case, the relevant art is semiconductor processing, and in semiconductor processing, the terms growing and depositing have different usages. One of ordinary skill in the art in semiconductor processing would turn to a treatise such as the Wolf and Tauber reference described above rather than a non-technical dictionary to determine the meanings of these words, which are clearly being used in a technical context. Furthermore, the Federal Circuit has repeatedly cautioned against the use of non-scientific dictionaries for defining technical words. See *AFG Industries, Inc. and Asahi Glass Company, Ltd. v. Cardinal IG Company, Inc. and Andersen Windows, Inc.*, 239 F.3d 1239, 1247-49 (Fed. Cir. 2001). That is, dictionary definitions of ordinary words are rarely dispositive of their meanings in a technological context. *Id* (citing *Anderson v. International Engineering & Manufacturing, Inc.*, 160 F.3d 1345, 1348-49 (Fed. Cir. 1998)). Accordingly, a technical term used in a patent is interpreted as having the meaning a person of ordinary skill in the field of the invention would understand it to mean. See *Dow Chemical*, 257 F.3d at 1372-73. Therefore, Appellants submit that the Examiner is incorrectly relying on the definition of "growing" as presented in a non-technical dictionary since "growing" has a different meaning as known in the relevant art and as used throughout the specification and claims, which is consistent with the descriptions of growing and depositing provided by the Wolf and Tauber technical treatise in the area of semiconductor processing.

Therefore, Applicants are requesting reinstatement of the previously-filed Appeal Brief and are providing the above arguments in response to the Examiner Office Action that reopened prosecution. For these additional reasons, reversal with respect to each of Groups A and B is requested.

Respectfully submitted,



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APPENDIX

1. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width and a second trench of a second width in the semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

forming a mask over the second trench;

etching at least a portion of the first insulator liner while the mask is over the second trench;

removing the mask; and

depositing an insulating layer in the first trench and the second trench.

2. The method of claim 1, wherein the first width is less than the second width.

3. The method of claim 1, wherein the step of etching comprises completely removing the first insulator liner.

4. The method of claim 1, wherein the step of etching results in leaving at least one hundred Angstroms of the first insulator liner.

5. The method of claim 1, wherein the step of growing the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

6. The method of claim 1, wherein the step of etching comprises dipping the semiconductor device structure in hydrofluoric acid.

7. The method of claim 1, wherein the step of etching comprises applying a dry etch chemistry to the semiconductor device structure.

8. The method of claim 1, wherein the insulator layer comprises high density plasma oxide fill.

9. The method of claim 1, further comprising forming a barrier layer and a stress relief layer over the semiconductor layer in areas adjacent to the first trench and the second trench.

10. The method of claim 1, further comprising forming a pad nitride and pad oxide over the semiconductor layer prior to forming the first trench and the second trench, and wherein the step of forming the first trench and the second trench comprises etching through selected portions of the pad nitride and the pad oxide and into the semiconductor layer.

15. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width and a second trench of a second width in the semiconductor layer, the first width being less than the second width;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

forming a mask over the second trench; and

etching at least a portion of the first insulator liner while the mask is over the second trench.

16. The method of claim 15, wherein the step of etching comprises a wet etch.

17. The method of claim 16, wherein the step of etching comprises dipping the semiconductor device structure in hydrofluoric acid.

18. The method of claim 15, wherein the etching comprises a dry etch.

19. The method of claim 15, wherein the step of growing the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

20. The method of claim 15, wherein:

the semiconductor layer has a top surface;

the second trench has a corner where the trench adjoins the top surface of the semiconductor layer; and

the step of growing the first insulator liner and the second insulator liner comprises rounding of the corner of the second trench.

21. The method of claim 20, wherein the corner is semiconductor.

22. The method of claim 15, wherein the step of etching comprises leaving at least 100 Angstroms of the first insulating liner.

23. The method of claim 15, wherein the step of etching comprises removing the first insulating liner.

24. The method of claim 15, further comprising forming a barrier layer and a stress relief layer over the semiconductor layer in areas adjacent to the first trench and the second trench.

25. The method of claim 24, wherein the barrier layer comprises nitride and the stress relief layer comprises oxide.

26. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width in the semiconductor layer;

forming a second trench of a second width greater than the first width in the second semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

etching a portion of the first insulator liner; and

depositing an insulating layer in the first trench.

27. The method of claim 26 further comprising

forming a mask over the second trench prior to the step of etching; and

removing the mask prior to the step of depositing.

28. The method of claim 26, wherein the step of etching further comprises etching a portion of the second insulator liner and leaves at least 50 Angstroms of the first insulator liner and 50 Angstroms of the second liner.

29. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width in the semiconductor layer;

forming a second trench of a second width in the second semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

etching a portion of the first insulator liner and a portion of the second insulator liner; and

depositing an insulating layer in the first trench and the second trench.

30. The method of claim 29, wherein the step of etching comprises a wet etch.

31. The method of claim 30, wherein the wet etch uses hydrofluoric acid.

32. The method of claim 29, wherein the first insulator and the second insulator liner comprises thermal oxide.

33. The method of claim 29, wherein the step of depositing comprises filling the first trench and second trench.

34. The method of claim 33, wherein the insulating layer comprises high density plasma oxide.

38. A method for forming a semiconductor device structure in a semiconductor layer having a top surface, comprising:

forming a first trench of a first width in the semiconductor layer and having a first corner at the surface of the semiconductor layer;

forming a second trench of a second width greater than the first trench in the second semiconductor layer and having a second corner at the surface of the semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench to achieve a radius of curvature of at least 200 Angstroms in the first and second corner;

etching a portion of the first insulator liner and a portion of the second insulator liner; and

depositing an insulating layer in the first trench and the second trench that fills the first and second trenches, wherein the insulating layer is free of voids.

39. The method of claim 38, wherein the first insulator liner and the second insulator liner are thermal oxide.

40. The method of claim 38, wherein the step of etching leaves the first insulator liner and the second insulator liner at a thickness sufficiently small to allow for completely filling the first trench with the insulating layer without voids in the insulating layer.

41. The method of claim 40, wherein the insulating layer comprises high density plasma oxide.

42. The method of claim 38, wherein the step of etching is further characterized as leaving at least 50 Angstroms of the first insulator liner and the second insulator liner.